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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,721	01/21/2004	Thomas James Fox	RPS920030082US1	3705

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EXAMINER	
LE, DIEU MINH T	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,721	FOX ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,12,15-20 and 23* is/are rejected.

7)☒ Claim(s) *2,3,10,11,13,14,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed 11/24/2006 in application 10/761,721.

2. Claims 1-23 are again presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 4-9, 12, 15-20, and 23 are again rejected under 35 U.S.C. 103(a) as being unpatentable over McKay et al. (U.S. 6,138,247 hereafter referred to as McKay) in view of Morikawa et al. (U.S. 5,898,829 hereafter referred to as Morikawa).

This rejection is being applied for the same reasons set forth in the previous Office Action mailed 08/23/2006.
As per claims 1, 4-9, 12, 15-20, and 23 see the previous office action for the detailed teaching of McKay and Morikawa as well as the motivation and reasons for combined.

Applicant asserts that McKay and Morikawa failed to teach or suggest the following:

A. an inactive (non-functioning) processor that does not process any workload (i.e., "said spare processor is not allocated any processing load by the operating system OS…);

B. (a) use of a processor register comprising bits, which indicate an active (operational) or inactive (in-operational) status of a corresponding/associated processor; (b) initially setting the bit corresponding to the spare processor to inactive, while setting the bits corresponding to the other processors to active; and (c) re-setting the bit of the spare processor to active and that of a failing processor to inactive when bringing the spare processor online;

C. an IA-32 architecture or functionality associated therewith;

D. continuously monitoring the status of operating processors, as provided by Applicant's claims.

Examiner respectfully transverses Applicant's argument as follows:

A. First, Examiner would like to bring Applicant attention to McKay's multiprocessors system configured for switching (i.e.,

fail-over) between multiprocessors [abstract, fig. 10, col. 2, lines 10-30] comprising ***a multi-system processor architectures including multi-configuration management function, examining and interruption enable management, seamless switching and continuity operation functions*** [col. 2, lines 30-35, col. 7, lines 1-7, col. 8, lines 1-30]. McKay clearly demonstrated and performed data failure detection and recovery (i.e., ***fail-over***) via plurality of processors by configuring and interrupting processes. In addition, Morikawa's fault tolerant computer system including active/backup multi-processors failure detection and correction [abstract, fig. 6, col. 1, claims 10-20] comprising ***an*** operational state information ***used in supporting the failover process [col. 21, lines 20-30] via a*** multi-configuration "watchdog" means ***[col. 5, lines 20-42]***. It is clear that both McKay and Morikawa do teach applicant's invention.

Second, in response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the feature upon which Applicant relies (i.e., ***an inactive (non-functioning) processor that does not process any workload***) is not recited in the rejected claim. Although the claim is interpreted in light of the specification,

limitations from the specification is not read into the claims. *In re Van Guens, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).*

Third, it is ***not*** true that both McKay and Morikawa failed to teach "the inactive (non-functioning) processor that does not process any workload". McKay explicitly illustrated that "when one of the operating processors is determined to be failing, dynamically (i.e., ***seamless switchover***) activating said spare processor to replace the failing operating processor, wherein the processing load of the failing processor is automatically sent to the spare processor for processing (i.e., ***fail-over process")*** [abstract, fig. 10, col. 2, lines 10-30, col. 6, lines 59 through col. 7, lines 14, col. 8, lines 20-31]. In addition, Morikawa demonstrated the fault tolerant computer system including active/backup multi-processors failure detection and correction [abstract, fig. 6, col. 1, claims 10-20] via ***the operational state information used in supporting the failover process*** [col. 21, lines 20-30].

Therefore, it is obvious to an ordinary skill in the art that the combination of the McKay and Morikawa's inventions do clearly teach applicant's limitation.

B. First, in response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the feature upon which Applicant relies (i.e., ***(a) use of a processor register comprising bits, which indicate an active (operational) or inactive (in-operational) status of a corresponding/associated processor; (b) initially setting the bit corresponding to the spare processor to inactive, while setting the bits corresponding to the other processors to active; and (c) re-setting the bit of the spare processor to active and that of a failing processor to inactive when bringing the spare processor online***) is not recited in the rejected claim. Although the claim is interpreted in light of the specification, limitations from the specification is not read into the claims. *In re Van Guens, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).*

Second, McKay explicitly addressed multiprocessor that includes a basic input/output system (BIOS) [col. 2, lines 30-47] and a processor register linked to said BIOS, which indicates which processors among said operating processors and said spare processors are currently available to said OS for allocating load, wherein said holding off of the spare processor comprises: setting a bit within said register corresponding to

each of said operating processors to an active state during said initial POST, wherein said active state indicates to said OS that the corresponding operating processor is available for allocating load; and setting a bit corresponding to said spare processor an inactive state. [fig. 10, col. 2, lines 10-30, col. 3, lines 30-53, col. 4, lines 32-50, col. 6, lines 10-35], wherein said dynamically activating step comprises: re-setting a bit corresponding to the failing processor to an inactive state; and setting said bit corresponding to said spare processor to an active state (i.e., ***seamless switchover***, ***fail-over process)*** [abstract, fig. 10, col. 2, lines 10-30, col. 4, lines 30-52, col. 6, lines 10-35, col. 6, lines 59 through col. 7, lines 14, col. 8, lines 20-31]. In addition, Morikawa explicitly demonstrated the fault tolerant computer system including active/backup multi-processors failure detection and correction [abstract, fig. 6, col. 1, claims 10-20] comprising ***an*** operational state information ***used in supporting the*** failover process ***[col. 21, lines 20-30] via a*** multi-configuration "watchdog" means ***(i.e.,*** using setting bit to performing this watchdog function***) [col. 5, lines 20-42].***

Therefore, it is obvious to an ordinary skill in the art that the combination of the McKay and Morikawa's inventions do clearly teach applicant's limitation.

C. It is ***not*** true that both McKay and Morikawa failed to teach "the IA-32 architecture or functionality associated therewith". **As indicate in previous office action that,** a person having ordinary skill in the art at the time of Applicant's invention to first realizing McKay's ***multi-system processor architectures including multi-configuration management function, examining and interruption enable management, seamless switching and continuity operation functions*** as being the MP configured according to IA-32 architecture as claimed by Applicant. This is because McKay's mutli-data processors /fault tolerant system explicitly performed data failure detection and recovery (i.e., ***fail-over***) via plurality of processors via configuration and interrupting processes. By utilizing these capabilities, the multi-data processing system can be directed or redirected promptly and functioned properly during failover switching process in supporting the system operation; second, by applying the ***operational state information*** used in supporting the failover process via a ***multi-configuration "watchdog"*** means as taught by Morikawa in conjunction with the multiprocessors system configured for switching (i.e., fail-over) between multiprocessors as taught by McKay, the multi-processors within fault tolerant networking system including backup capability (i.e., failover) can enhance its operation performance, more

specifically to ensuring the error detected, corrected, and replaced (i.e., backup) in proper and efficient manner via its state information functionality.

Therefore, it is obvious to an ordinary skill in the art that the combination of the McKay and Morikawa's inventions do clearly teach applicant's limitation.

D. First, in response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the feature upon which Applicant relies (i.e., ***continuously monitoring the status of operating processors, as provided by Applicant's claims***) is not recited in the rejected claim. Although the claim is interpreted in light of the specification, limitations from the specification is not read into the claims. *In re Van Guens, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).*

Second, McKay explicitly addressed multiprocessors system configured for switching (i.e., fail-over) between multiprocessors [abstract, fig. 10, col. 2, lines 10-30] comprising ***a multi-system processor architectures including multi-configuration management function, examining and interruption enable management, seamless switching and***

continuity operation functions [col. 2, lines 30-35, col. 7, lines 1-7, col. 8, lines 1-30]. In addition, Morikawa's fault tolerant computer system including active/backup multi-processors failure detection and correction [abstract, fig. 6, col. 1, claims 10-20] comprising ***an*** operational state information ***used in supporting the failover process [col. 21, lines 20-30] via a*** multi-configuration "watchdog" means ***[col. 5, lines 20-42]***. It is clear that both McKay and Morikawa do teach applicant's invention.

Therefore, it is obvious to an ordinary skill in the art that the combination of the McKay and Morikawa's inventions do clearly teach applicant's limitation.

Allowable Subject Matter

5. Claims 2-3, 10-11, 13-14, 21-229 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's arguments filed 11/24/2006 have been fully considered but they are not persuasive.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644.
The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

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